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updated

INTERCONNECTION RESOURCES FOR  
PROGRAMMABLE LOGIC INTEGRATED  
CIRCUIT DEVICES

This is a continuation of U.S. patent  
5 application No. 10/299,572, filed November 18, 2002, *is now a U.S. patent  
6,727,727* which is a continuation of U.S. patent application No. 10/017,199, filed December 14, 2001 (issued as U.S. Patent No. 6,525,564, February 25, 2003), which is a continuation of U.S. patent application No. 09/517,146, 10 filed March 2, 2000 (issued as U.S. Patent No. 6,366,120, April 2, 2002), which claims the benefit of the following U.S. provisional patent applications: No. 60/122,788, filed March 4, 1999; and No. 60/142,431, filed July 6, 1999. All of these prior applications 15 are hereby incorporated by reference herein in their entireties.

Background of the Invention

This invention relates to programmable logic array integrated circuit devices ("programmable logic devices" or "PLDs"), and more particularly to 20 interconnection resources for use on programmable logic devices that increase the speed at which those devices can be made to operate.

Programmable logic devices typically include 25 (1) many regions of programmable logic, and (2)